Abstract:

Please amend the abstract by rewriting as shown below with underlining corresponding to additions and strikeouts corresponding to deletions.

ABSTRACT

~~With typical memory controllers, transactions over a data bus are performed serially. Therefore, there can be clock cycles between transactions for which the data bus is unnecessarily idle. By performing transactions concurrently, the number of idle clock cycles between transactions can be reduced.~~ An embodiment of a bus management device permits scheduling of transactions to allow concurrent execution of the transactions. Data bus usage is scheduled by setting shift register bits. Each position in the shift register corresponds to one clock cycle. When a current transaction is in a data phase, the value in the shift register is used to determine when to begin a control phase of the next transaction so that a desired number of idle clock cycles are present between data bus usage time periods for successive transactions. ~~That is, the control phase of the next transaction is started so that valid data is present on the data bus during the clock cycle corresponding to the beginning of the data phase for that transaction as specified by the bits in the shift register. By using the shift register to schedule usage of the data bus, the likelihood of bus contention is reduced. In addition, in a system using memory devices having different latency time periods, scheduling of the usage of the data bus so that the desired number of idle clock cycles between successive time periods of data bus usage is easily accomplished.~~

A2